**Amendments to the CLAIMS:**

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

**LISTING OF CLAIMS:**

1. (Previously Presented) An apparatus comprising:

a voltage regulation module coupled to an integrated circuit die having an exposed surface layer, the voltage regulation module including:

an interposer layer including voltage regulator elements, the interposer layer having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked surface-to-surface with the exposed surface layer; and

interconnect elements adapted to couple the interposer layer to the integrated circuit die.

2. (Previously Presented) The apparatus of claim 1, wherein the interposer layer is thinned to enable thru-vias to penetrate completely through the interposer.

3. (Previously Presented) The apparatus of claim 1, wherein the voltage regulator elements include both linear regulator elements and switching regulator elements, the linear regulator elements being situated to provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

4. (Previously Presented) The apparatus of claim 3, further comprising:

passive circuit elements, the passive circuit elements including at least one of metal-insulator metal capacitors and high-bandwidth inductors.

5. (Previously Presented) An apparatus comprising:

a voltage regulation module directly coupled to an exposed surface layer of an integrated circuit die including:

a two-dimensional hybrid array of voltage regulator elements, the voltage regulator elements including a minority of linear regulator elements and a majority of switching regulator elements, the two-dimensional array converting a

supply voltage into a regulated voltage and providing the regulated voltage to the integrated circuit die;

wherein the minority of linear regulator elements supply regulated voltage to areas on the integrated circuit die that intermittently demand high current levels.

6. (Previously Presented) The apparatus of claim 5, wherein the two-dimension hybrid array is embedded in an interposer adapted to interface two-dimensionally with the exposed surface layer.

7. (Previously Presented) The apparatus of claim 6, further comprising:

thru-vias penetrating through and insulated from the interposer, the thru-vias being adapted to connect the exposed surface of the integrated circuit die with a substrate.

8. (Previously Presented) The apparatus of claim 6, wherein the hybrid array of voltage regulator elements includes both linear regulator elements and switching regulator elements, the linear regulator elements being situated to interface with and provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

9. (Previously Presented) The apparatus of claim 8, further comprising:

passive circuit elements, the passive circuit elements including at least one of metal-insulator metal capacitors and high-bandwidth inductors.

10. (Currently Amended) A system comprising:

a power supply;

a substrate coupled to the power supply;

an integrated circuit die having an exposed circuit side; and

an interposer situated between the substrate and the integrated circuit die, the interposer having voltage regulator elements for receiving voltage from the power supply and for down-converting the voltage from the power supply into a regulated voltage, the interposer delivering the regulated voltage to the integrated circuit die;

wherein the voltage regulator elements include a minority of linear regulator elements and a majority of switching regulator elements.

11. (Previously Presented) The system of claim 10, wherein the interposer and the exposed circuit side of the integrated circuit die are bonded in a flip-chip fashion.

12. (Previously Presented) The system of claim 11, further comprising:

thru-vias penetrating through and insulated from the interposer, the thru-vias being connecting the exposed circuit side of the integrated circuit die directly to the substrate;

wherein the interposer includes a circuit side coupled to the exposed circuit side of the integrated circuit die with short solder ball elements, and a reverse side coupled to the substrate with interconnect elements.

13. (Currently Amended) The system of claim 11, wherein ~~the interposer includes a hybrid array of voltage regulator elements, the hybrid array of voltage regulator elements including both linear regulator elements and switching regulator elements,~~ the linear regulator elements ~~being~~ are situated to provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

14. (Previously Presented) A method comprising:

coupling an array of distributed low bandwidth and high bandwidth voltage regulators surface-to-surface to an integrated circuit die;

determining locations of hot spots on the integrated circuit die; and

placing the high bandwidth voltage regulators on locations of the array corresponding to the hot spot locations on the integrated circuit die.

15. (Previously Presented) The method of claim 14, further comprising:

minimizing interconnect distances between the voltage regulators and the integrated circuit die.

16. (Previously Presented) The method of claim 15, further comprising:

embedding the array of distributed high bandwidth and low bandwidth voltage regulators in an interposer having a circuit side and a reverse side;

bonding the circuit side of the interposer to the integrated circuit die in a flip-chip fashion; and

coupling the reverse side of the interposer to a substrate coupled to a power supply.

17. (Previously Presented) The method of claim 14, wherein the high bandwidth voltage regulators are linear regulators, and the low bandwidth voltage regulators are switching regulators.

18. (Previously Presented) The method of claim 15, wherein solder ball elements interconnect the interposer and the integrated circuit die.

19. (Previously Presented) The method of claim 15, wherein copper-to-copper interconnects couple the interposer and the integrated circuit die.

20. (Previously Presented) The method of claim 16, further comprising:

coupling the integrated circuit die directly to the substrate with insulated thru-vias passing through the interposer.